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Adaptive Logic Circuits with Doping-Free Ambipolar Carbon Nanotube Transistors

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Received October 9, 2008; Revised Manuscript Received February 2, 2009

ABSTRACT

A CMOS-like inverter was integrated by using ambipolar carbon nanotube (CNT) transistors without doping. The ambipolar CNT transistors automatically configure themselves to play a role as an n-type or p-type transistor in a logic circuit depending on the supply voltage (V_{DD}) and ground. A NOR (NAND) gate is adaptively converted to a NAND (NOR) gate. This adaptiveness of logic gates exhibiting two logic gate functions in a single logic circuit offers a new opportunity for designing logic circuits with high integration density for next generation applications.

Single-walled carbon nanotubes (SWCNTs) provide an opportunity to achieve extremely high intrinsic carrier mobility and high current carrying capacity.1–6 However, several obstacles with their use have been encountered. Among them, ambipolarity in Schottky barrier carbon nanotube field effect transistors (CNT-FET) is a well-known phenomenon occurring under a vacuum environment or with a top gate oxide and top gate electrode.7,8 CNT-based CMOS technology has been realized by suppressing one of the ambipolar regions of the CNTs with p- or n-type doping.9–20 These approaches are limited to the conventional concept of silicon devices that utilize unipolar p- and n-type transistors in the realization of CMOS. Doping of CNTs with p- or n-type to remove ambipolarity is still challenging. Here, we report a different approach that considers ambipolarity not as a drawback but as a benefit in architecturing CNT-based CMOS circuits. CMOS-like logic circuits such as inverters and NOR/NAND gates were integrated by using ambipolar CNT transistors without the use of an unreliable doping process. The key idea in this work is that ambipolar CNT transistors automatically configure themselves to play the role as n-type or p-type transistors in logic circuits depending on the exchange of the supply voltage (V_{DD}) and ground. As a proof of concept, we demonstrate that by flipping the voltage of V_{DD} and ground, a NOR (NAND) gate can be adaptively converted to a NAND (NOR) gate. This adaptiveness of logic gates exhibiting two logic gate functions by using one logic circuit has never been demonstrated.

An array of thin film transistors (TFTs) was fabricated with randomly networked single-walled carbon nanotubes (SWCNTs) that were synthesized selectively on a designed array of catalyst photoresists (0.01 M of ferrocene)21 by using a remote plasma-enhanced chemical vapor deposition (PECVD) method at low temperature (450 °C).22 The corresponding source and drain electrodes with Ti (5 nm)/Au (50 nm) (channel length, 2, 3, 5, 7, 10 µm; width, 40 µm; 20 channels for each length in a sample) were deposited to form an array of 200 TFTs. A conformal thin film of a top gate oxide (Al_{2}O_{3}, 50 nm) was deposited by an atomic layer deposition technique at 150 °C. The gate electrode (Ti (5 nm)/Au (50 nm)) was formed similarly to the source and drain electrodes. The detailed method has been described elsewhere.21,22 Logic circuits were fabricated by connecting several TFTs with gold wire with wire bonder.

I–V characteristics of the CNT-TFTs were measured under ambient conditions by a source-measure unit (Keithley 236, 237) using a probe station. Gate biases of −40 to +40 V were applied for back gate measurements and a top gate voltage of −5 to +5 V was applied at a source and drain bias of 100 mV. Scanning electron microscopy (JEOL, JSM-
7401F) images were taken by secondary electron image mode under a pressure of \( \sim 4 \times 10^{-3} \) Torr.

Although isolated SWCNT-FETs are mostly desired to demonstrate adaptive logic circuits with ambipolar transistors, an array of SWCNT thin film transistors (TFTs) was chosen in this study. Recently, SWCNT-based network TFTs are of interest for application in flexible electronics. The concept considered here is even more relevant to isolated SWCNT-FETs. Figure 1a illustrates the schematic of a top-gate SWCNT network TFT. Optical images of an array of top-gate TFTs (Figure 1b) and a typical scanning electron microscopy (SEM) image of a SWCNT network in the channel area (Figure 1c) are also shown. A sub-monolayer SWCNT (\( \sim 25 \) tubes/\( \mu \)m\(^2\)) network was synthesized between the source and drain electrodes. In each sample, 200 TFTs were fabricated with different channel lengths varying from 2 to 10 \( \mu \)m.

The yield of working electrodes was 88\%, and their mobilities were \( \sim 8 \) cm\(^2\)/(V\cdot s). The backgate test showed that 94\% of the connected TFTs had an on/off ratio \( >10^4 \) and 66\% had an on/off ratio \( >10^5 \) (Figure 1d). The main reason for the high on/off ratios observed here is the abundance of semiconducting SWCNTs synthesized by remote PECVD, which has been reported previously. The on/off ratio was also improved with increasing channel length (Figure 1e,f). Even though some metallic CNTs were retained in the sample, the probability of having semiconducting channels in the network transistor increased with the channel length. Because of this, our network TFTs showed a higher percentage of semiconducting transistors (94\%, on/off ratio of \( >10^4 \) than the isolated SWCNT transistors (89\%\)).

Device failure (disconnected device) was more abundant at longer channel lengths. The demonstration of network TFTs with a high yield and controllability of semiconducting transistors opens the possibility for this approach to be utilized in sophisticated CNT-based circuits.

Figure 2a shows \( I-V \) characteristics of a typical ambipolar CNT transistor. Unlike p-type transistors obtained under ambient conditions, our top-gate TFTs had a high yield of ambipolarity of \( >90\% \). With a negative gate bias, the conduction and valence bands of the CNTs were upshifted to generate hole carriers. On the other hand, with a positive gate bias, the conduction and valence bands were downshifted to generate electron carriers. Thus, hole and electron currents were generated depending on the gate bias. This unique behavior has been a serious drawback compared to Si technology in which only one type of carrier is dominant to operate the device. For this reason, unipolar CNT
transistors have been contrived by intentional doping techniques.\textsuperscript{9–20} However, we demonstrate that the ambipolarity in CNTs is not a drawback but can be an advantage in fabricating logic circuits.

As proof of concept, we fabricated an inverter with two ambipolar CNT transistors (Figure S1 in Supporting Information and Figure 2b). A $V_{DD}$ of +5 V applied to the source of Tr1 is equivalent to −5 V to the gate, relative to the source, and thus, the effective gate bias of Tr1 is shifted by −5 V in the $I$–$V$ characteristics (Figure 2c). On the other hand, the source in Tr2 is grounded and there is no voltage difference with the gate. Therefore, the gate bias is not shifted in the $I$–$V$ characteristics. Under this circumstance, if a $V_{in}$ (gate) between 0 and 5 V is applied, the hole current dominates in Tr1 due to the effective gate bias shift, as shown in the inset of Figure 2d, and the electron current dominates in Tr2. As a consequence, the typical CMOS inverter was formed similarly to the doped silicon device. A clear switching effect was observed by controlling $V_{in}$ between 0 and 5 V (Figure 2d). The output high level (4–5 V) and low level (~0 V) were close to that of the isolated doped SWCNT inverter and the gain was 4, similar to the Si device level (4–8) (Figure S2 in Supporting Information).\textsuperscript{14} Unlike the Si device in which each device type is predetermined, an ambipolar CNT-based inverter utilizes the intrinsic semiconductor and, more importantly, each device type is determined by the signs of $V_{in}$ (gate bias), source bias, and drain bias where the changes of the band diagram of the related devices are illustrated in Figure 2d. With $V_{in} = 0$ V ($V_{out} = 5$ V), Tr1 becomes a p-type on-state and Tr2 becomes an intrinsic off-state, whereas with $V_{in} = 5$ V ($V_{out} = 0$ V) applied, Tr2 becomes an n-type on-state and Tr1 becomes

Figure 2. (a) Transfer characteristics of ambipolar transistor and the corresponding band diagrams for various gate voltages (inset). (b) Schematic view of inverter with two ambipolar transistors (left) and circuit diagram (right). Inverter circuit diagram and transfer characteristic shift of each transistor with (c) $V1 = V_{DD}$ and $V2 = $ ground (GND) and (e) $V1 = $ GND and $V2 = V_{DD}$. Inverter characteristics (d) (red circles) and gain (blue circles) and band diagram (f) of two ambipolar transistors with $V_{in} = 0$ V and $V_{out} = 5$ V (left), and $V_{in} = 5$ V and $V_{out} = 0$ V (right) for each (c) and (e) case.
an intrinsic off-state. An intriguing effect was observed when an opposite direction of $V_{DD}$ was applied, i.e., $V_{DD}$ of 5 V to the source of Tr2 and ground to the source of Tr1 (Figure 2e). In this case, Tr2 behaves as a p-type and Tr1 behaves as an n-type by the similar principle described previously. A clear switching characteristic was obtained again by controlling $V_{in}$ between 0 and 5 V (Figure 2f), despite the conversion of the types of the two transistors.

The most intriguing outcome of this work is the adaptiveness in integrating CMOS-like logic gates using ambipolar SWCNT TFTs. Figure 3a shows a logic gate using four ambipolar TFTs. The NOR gate was realized when a $V_{DD}$ of 4 V was applied to the source of Tr1 and ground to the source of Tr2 and Tr4. In this case, Tr1 and Tr3 behave as p-type transistors and Tr2 and Tr4 behave as n-type transistors, following the above inverter principle (Figure S3a in Supporting Information). By combining $V_A$ and $V_B$, a NOR function was obtained, as shown in Figure 3b. The adaptiveness of this logic gate was demonstrated by flipping $V_{DD}$ and ground, i.e., a $V_{DD}$ of 4 V was applied to the source of Tr2 and Tr4 and ground to the source of Tr1. When the same bias combinations of $V_A$ and $V_B$ are applied, a NAND function was achieved. In this case, Tr1 and Tr3 behaved as n-type transistors and Tr2 and Tr4 behaved as p-type transistors, which is the opposite of the NOR gate (Figure S3b in Supporting Information). We emphasize that two functions of NOR and NAND gates were realized by using one set of logic gates. The high drain–source bias used here generated the leakage current that gave rise to ambiguous on and off states (Figure S4 in Supporting Information). The leakage current could be minimized by forming a thin oxide layer. The demonstrated adaptive logic gate with ambipolar transistors provide several advantages in designing multifunctional logic circuits with a simplified fabrication process and, moreover, in improving integration density. This should open up new avenues in realizing nanotube-based electronic devices in the near future.

Despite excellent advantages of ambipolar transistor in fabricating inverter and logic circuit, several difficulties arise particularly in the case of random network CNT-FETs. The values of $V_{in}$ and $V_{out}$ should be similar to each other. This requires several control variables such as threshold voltage, the current levels of on and off states, hysterisis, and on/off ratio. The control of transistor characteristics of individual CNT transistors is essential to fabricate complex logic circuits. Another issue in the flipping supply bias takes place in particular complex circuits such as adder and multiplier. New concept of wiring is required to realize such complex circuits. The probable use of the adaptive logic circuit is, for instance, the $S$–$R$ latch that consists of two NOR gates and the $S$–$R$ latch that consists of two NAND gates. The conventional CMOS process requires two latches separately. However, in the case of using our adaptive logic circuits, only one $S$–$R$ latch is required and the counterpart $S$–$R$ latch can be obtained by flipping the $V_{DD}$ and ground. Our adaptive logic circuits will be useful for simple hardware programs in portable electronics that require space saving, low power consumption, and high speed.
Acknowledgment. This work was supported by the KRFG funded by the Korean Government (MOEHRD, Basic Research Promotion Fund) (KRF-2005-084-C00014), the TND project, the WCU program through the KOSEF funded by the MEST (R31-2008-000-10029-0), the KICOS through a grant provided by MOST in 2007 (No. 2007-00202), and KOSEF through CNNC at SKKU.

Supporting Information Available: Transfer characteristics of two ambipolar transistors which were used to inverter (S1), $V_{IN}-V_{OUT}$ characteristics of CMOS inverter (S2), operation voltages of ambipolar CMOS inverter (T1), and logic circuit diagram and transfer characteristic shift of each transistor (S3). This material is available free of charge via the Internet at http://pubs.acs.org.

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